

CLAIMS

What is claimed is:

- 1 1. A method, comprising:  
2 determining that each thread running on a processor has issued a pause  
3 instruction; and  
4 reducing power consumption in response to the determination that each  
5 thread running on the processor has issued a pause instruction.  
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- 1 2. The method of claim 1, further comprising reducing the frequency of the  
2 processor.  
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- 1 3. The method of claim 1, further comprising gating M clock cycles out of every  
2 N clock cycles of a processor clock.  
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- 1 4. The method of claim 1, further comprising increasing power consumption after  
2 a predetermined time period has elapsed or when an event occurs.  
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- 1 5. The method of claim 1, further comprising lowering processor voltage.  
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- 1 6. The method of claim 1, further comprising running only one thread on the  
2 processor.  
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- 1 7. The method of claim 1, further comprising slowing down the processor.  
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- 1 8. A method, comprising:  
2 determining that each thread running on a processor has issued a pause  
3 instruction; and  
4 leave a normal mode of operation and entering into a slow mode of  
5 operation in response to the determination that each thread running on the processor  
6 has issued a pause instruction.  
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- 1 9. The method of claim 8, further comprising reducing processor frequency.  
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- 1 10. The method of claim 8, further comprising gating M clock cycles out of every  
2 N clock cycles of a processor clock.  
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- 1 11. The method of claim 8, further comprising returning to the normal mode of  
2 operation after a predetermined time period has elapsed.  
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- 1 12. The method of claim 8, further comprising returning to the normal mode of  
2 operation when an event occurs.  
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- 1 13. The method of claim 8, further comprising running only one thread on the  
2 processor.  
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- 1 14. The method of claim 8, further comprising lowering processor voltage.  
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- 1 15. The method of claim 8, further comprising loading counters associated with the  
2 threads with a value to indicate how long the associated thread is to remain paused.  
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1 16. The method of claim 8, further comprising leaving the slow mode of operation  
2 and entering a slower mode of operation in response to a determination that the  
3 processor has been in the slow mode for a predetermined time period.

1 17. A method, comprising:  
2 receiving a pause instruction from each thread running on a processor;  
3 and  
4 hinting the processor to enter a low power mode in response to receiving  
5 the pause instruction from each thread running on the processor.

1 18. The method of claim 17, further comprising hinting the processor to remain in  
2 the low power mode for a predetermined time period.

1 19. The method of claim 17, further comprising hinting the processor to remain in  
2 the low power mode until an event occurs.

1 20. The method of claim 17, further comprising hinting the processor to enter a  
2 lower power mode after a predetermined time period elapses.

1 21. The method of claim 17, further comprising reducing a processor clock  
2 frequency.

1 22. The method of claim 17, further comprising lowering a processor voltage.

1 23. The method of claim 17, further comprising gating M clock cycles out of every  
2 N clock cycles of a processor clock.

1 24. An article of manufacture including a machine-accessible medium having data  
2 that, when accessed by a machine, cause the machine to perform the operations  
3 comprising:

4 receiving a pause instruction from each thread running on a processor;  
5 and

6 hinting the processor to enter a low power mode in response to receiving  
7 the pause instruction from each thread running on the processor.  
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1 25. The article of manufacture of claim 24, wherein the machine-accessible  
2 medium further includes data that cause the machine to perform operations comprising  
3 hinting the processor to remain in the low power mode for a predetermined time  
4 period.  
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1 26. The article of manufacture of claim 24, wherein the machine-accessible  
2 medium further includes data that cause the machine to perform operations comprising  
3 hinting the processor to remain in the low power mode until an event occurs.  
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1 27. The article of manufacture of claim 24, wherein the machine-accessible  
2 medium further includes data that cause the machine to perform operations comprising  
3 hinting the processor to enter a lower power mode after a predetermined time period  
4 elapses.  
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1 28. The article of manufacture of claim 24, wherein the machine-accessible  
2 medium further includes data that cause the machine to perform operations  
3 comprising reducing a processor clock frequency.  
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1 29. The article of manufacture of claim 24, wherein the machine-accessible medium  
2 further includes data that cause the machine to perform operations comprising lowering a  
3 processor voltage.

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1 30. The article of manufacture of claim 24, wherein the machine-accessible  
2 medium further includes data that cause the machine to perform operations comprising  
3 gating M clock cycles out of every N clock cycles of a processor clock.